CONFIGURABLE DELAY LINE CIRCUIT

ABSTRACT OF THE DISCLOSURE

A configurable circuit consistent with certain embodiments has a variable length delay line (10), the delay line (10) having an input (24) and having N delay elements (12, 14, 16, 18,..., 20) to provide a plurality of N delayed outputs (T(0) through T(N)). The variable length delay line (10) also has a number of active delay elements determined by a program command. A configurable processing array (32) receives the delayed outputs from the active delay elements and secondary data (38). The configurable processing array has an array of configurable circuit elements (104, 130, 150). The configurable processing array is configured to process the delayed outputs and the secondary data (38) in a manner for which the invention is to be used. This abstract is not to be considered limiting, since other embodiments may deviate from the features described in this abstract.